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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,223	LIM ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on January 30, 2003 was filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The disclosure is objected to because of the following informalities: missing Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention. Appropriate correction is required.

3. Claims 5 and 8 are objected to because of the following informalities: the acronyms PVT and IC in the respected claims should be identified explicitly at least once in the body of the claims to avoid potential confusion from unintended representations. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Re Claims 1-5, 9-13, 18-20

5. Claims 1-5, 9-13, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sevalia et al., U.S. Patent 6356122, hereinafter Sevalia.

6. In re claim 1, Sevalia discloses a timing circuit [fig.2; col.1, ll.65-66] comprising:

- At least one driving circuit [multiplexer] outputting an output signal [col.3, l.10; col.4, ll.31-32].
- A phase locked loop [conventional PLL] receiving a reference clock signal [ref clock from input pin] and supplying an output clock signal [signal from post divider M] to said at least one driving circuit, said phase locked loop generating said output clock signal according to said received reference clock signal and a feedback clock signal [fig.2; col.1, ll.56-64].
- First and second delay elements [programmable delays DL1 and DL2] located in the path of said reference clock path and the path of said feedback clock path, respectively, said first and second delay elements being configured to provide a delay in order to make said output signal meet a predetermined valid data timing requirement [fig.2; col.3, ll.12-24, ll.30-39; l.64 -- col.4, l.27; output is in phase with input for data timing to be valid].

7. As to claims 2 and 10, Sevalia discloses the delay elements [programmable delays DL1 and DL2] that are located only in the reference clock and feedback clock paths [fig.2].

8. As to claims 3 and 11, Sevalia discloses the first and second delay elements that are self-calibrating delay cells [col.4, ll.5-17, ll.39-40, l.50; one time programming of estimated delay subsequently lets delay circuits to calibrate or tune accordingly to be in phase].

9. As to claims 4, 12 and 19, Sevalia discloses the self-calibrating delay cells that calibrate themselves to meet specified timing adjustment, granularity and/or range [col.3, ll.40-63; col.4, ll.5-17, ll.39-40, l.50; transistors and other elements have rated performance specifications that are selected to be within a tolerable range for timing adjustment].

10. As to claims 5, 13, and 20, Sevalia discloses the self-calibrating delay cells that use a digital compensation technique to reduce PVT variations [col.3, ll.52-59; col.4, ll.17-20, ll.45-54; configuration bits digitally set values to compensate for PVT variations, taking into account the PVT characteristics of the delay elements].

11. In re claim 9, Sevalia discloses an I/O circuit [col.1, ll.56-59] comprising:

- A transmitting device [fig.2] outputting at least one output signal [multiplexer outputs one signal], said transmitting device having:
- At least one driving circuit [multiplexer], the number of driving circuits corresponding to the number of output signals [fig.2; col.3, l.10; col.4, ll.31-32].
- A phase locked loop [conventional PLL] receiving a reference clock signal [ref clock from input pin] and supplying an output clock signal [signal from post divider M] to said at least one driving circuit, said phase locked loop generating said output clock signal

according to said received reference clock signal and a feedback clock signal [fig.2; col.1, ll.56-64].

- First and second delay elements [programmable delays DL1 and DL2] located in the path of said reference clock path and the path of said feedback clock, respectively, said first and second delay elements being configured to provide a delay in order to make said output clock signal meet a predetermined valid data timing requirement [fig.2; col.3, ll.12-24, ll.30-39; l.64 -- col.4, l.27; output is in phase with input for data timing to be valid].
- A receiving device [col.2, ll.19-25] receiving said at least one output signal from said transmitting device, the timing of said received at least one output signal meeting said predetermined valid timing requirement [col.4, ll.17-20; configuraton set up for device to get in phase signals in order to operate correctly].

12. In re claim 18, Sevalia discloses a method of transferring a signal from a transmitting device [fig.2] to a receiving device [col.2, ll.19-25; circuit of fig.2 transmits clock signal to the device that the configurations are set to ensure timing is in phase] comprising:

- Outputting said signal from said transmitting device using a driving circuit [multiplexer] [col.3, l.10; col.4, ll.31-32].
- Receiving a reference clock signal in said transmitting device [fig.2; ref clock from input pin].
- Generating an output clock signal according to said received reference clock signal and a feedback clock signal in a phase locked loop [conventional PLL; col.1, ll.56-64].

- Providing a delay in a path of said reference clock signal and a path of said feedback clock signal [programmable delay DL1 and DL2], respectively, said delay being configured to make said at least one output signal meet a predetermined valid data timing requirement [col.3, ll.12-24, ll.30-39, l.64 -- col.4, l.27; output is in phase with input for data timing to be valid].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 6, 14

14. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia as applied to claims 5 and 13 above, and further in view of Hamza, U.S. Patent 5818270.

15. In re claims 6 and 14, Sevalia discloses every limitation of the claim as discussed above in reference to claims 5 and 13. Sevalia did not discuss utilizing a multi-tap delay buffer to delay a clock signal.

16. Hamza discloses a timing circuit [clock multiplier 10] that utilizes a multi-tap delay buffer [logical multiplier 14] in the clock signal [waveform 13] path to delay the clock signal, the amount of delay being controlled by selecting a tap of the multi-tap delay buffer [col.2, ll.41-60].

17. It would have been obvious to one of ordinary skill in the art, having the teachings of Savalia and Hamza before him at the time the invention was made, to modify the timing circuit taught by Savalia to include the multi-tap delay buffer as taught by Hamza, in order to obtain the

timing circuit wherein the digital compensation technique utilizes a multi-tap delay buffer in the feedback clock signal path to delay the feedback clock signal with the amount of delay being controlled by selecting a tap of the multi-tap delay buffer. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to contribute to the reduction of power and PVT variations [particularly the temperature] [Hamza: col.1, ll.37-39].

Re Claims 7-8, 15

18. Claims 7-8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia as applied to claim 1 above, and further in view of Byrn et al., U.S. Patent 5977837, hereinafter Byrn.

19. In re claims 7 and 15, Sevalia discloses every limitation of the claim as discussed above in reference to claim 1. Sevalia did not discuss the timing circuit comprising a plurality of driving circuits.

20. Byrn discloses a timing circuit [phase selector circuit 200] comprising a plurality of driving circuits [external frequency dividers 204, 206, and 208] and a phase locked loop [202] providing an output clock signal [PLL out] to all of the plurality of driving circuits [fig.2; col.2, ll.54-62].

21. It would have been obvious to one of ordinary skill in the art, having the teachings of Savalia and Byrn before him at the time the invention was made, to modify the timing circuit taught by Savalia to include the plurality of driving circuits as taught by Byrn, in order to obtain the timing circuit with the plurality of driving circuits for outputting a plurality of clock signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to output a plurality of clock signals.

22. As to claim 8, Byrn discloses the plurality of driving circuits that drive respective output signals from an IC chip [CMOS microprocessor] [col.1, ll.15-18; external is relative to the synchronization path].

Re Claims 16-17

23. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevalia as applied to claim 9 above, and further in view of Goldrian, U.S. Patent 5742798.

24. In re claim 16, Sevalia discloses every limitation of the claim as discussed above in reference to claim 9. Sevalia did not disclose expressly the I/O circuit operating with a bus.

25. Goldrian discloses an I/O circuit [fig.2] wherein the transmitting device [clock generator 200] and the receiving device [chip-A 204] comprise IC chips and the output signals [201] are driven on a bus [bus comprises of lines 201-203] between the IC chips [col.3, ll.27-54].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Salvalia and Goldrian before him at the time the invention was made, to use the IC chip-bus setting as taught by Goldrian for the I/O circuit disclosed by Salvalia as the setting taught by Goldrian is suitable for use with the I/O circuit of Salvalia. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase processing efficiency [col.1, ll.14-28].

27. As to claim 17, Goldrian discloses the transmitting device and the receiving device are mounted at a distance from each other on a printed circuit board [col.1, l.11].

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Millar, U.S. Patent 6337590, discloses a digital compensated locked loop.
- Nozawa, U.S. Patent 6014177, discloses a timing circuit with a driving circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
July 11, 2004

RERANA PERVEEN
PRIMARY EXAMINER